What is claimed is:

1. A method of forming a bit line contact hole, comprising:

providing a substrate having a transistor thereon, wherein the transistor comprises a gate layer covered by a first insulating layer, and a doped region;

forming a polysilicon layer to conformally cover the substrate and the transistor;

defining the polysilicon layer to form an inner landing pad connecting with the doped region;

conformally forming a passivation layer on the inner landing pad, the transistor, and the substrate;

forming a second insulating layer with a flat surface on the passivation layer;

forming a contact hole in the second insulating layer and the passivation layer to expose the inner landing pad; and

filling a metal layer in the contact hole.

2. The method as claimed in claim 1, wherein the thickness of the polysilicon layer is about 100~400Å.

3. The method as claimed in claim 1, wherein the polysilicon layer is defined by wet etching.

4. The method as claimed in claim 3, wherein an etching agent of etching polysilicon comprises an HF solution.

5. The method as claimed in claim 4, wherein the etching agent comprises NH_4F and HF of about 400~500:1.

6. The method as claimed in claim 1, the material of the passivation layer comprises silicon nitride.

7. The method as claimed in claim 1, wherein the thickness of the passivation layer is about 110~130Å.

8. The method as claimed in claim 1, wherein the second insulating layer is a stacked layer comprising a boro-phospho silicate glass (BPSG) layer and a tetraethylorthosilicate (TEOS) layer.

9. The method as claimed in claim 8, wherein formation of the BPSG comprises depositing a BPSG material on the passivation layer and polishing the BPSG material until the passivation layer is exposed.

10. The method as claimed in claim 8, wherein the thickness of the BPSG layer is about 5900~7300Å, and the thickness of the TEOS layer is about 3600~4400Å.

11. The method as claimed in claim 1, wherein the material of the metal layer comprises tungsten (W).

12. A method of forming a bit line contact hole, suitable for a substrate having a transistor thereon and comprising a memory cell array area and a logic circuit area, the transistor comprising a gate layer covered by a first insulating layer and a doped region, comprising:

forming a polysilicon layer to conformally cover the substrate and the transistor;

defining the polysilicon layer to form an inner landing pad connecting with the doped region in the memory cell array area;

conformally forming a passivation layer on the inner landing pad, the transistor, and the substrate;

forming a second insulating layer with a flat surface on the passivation layer;

forming a first contact hole, a second contact hole, and a third contact hole in the second insulating layer and the passivation layer, wherein the first contact hole exposes the surface of the inner landing pad in the memory cell array area, the second contact hole exposes the gate layer of the transistor in the logic circuit area, and the third contact hole exposes the doped region of the transistor in the logic circuit area; and

filling a metal layer in the first contact hole, the second contact hole, and the third contact hole.

13. The method as claimed in claim 12, wherein the thickness of the polysilicon layer is about 100~400Å.

14. The method as claimed in claim 12, wherein the polysilicon layer is defined by wet etching.

15. The method as claimed in claim 14, wherein an etching agent of etching polysilicon comprises an HF solution.

16. The method as claimed in claim 15, wherein the etching agent comprises NH_4F and HF of about 400~500:1.

17. The method as claimed in claim 12, the material of the passivation layer comprising silicon nitride.

18. The method as claimed in claim 12, wherein the thickness of the passivation layer is about 110~130Å.

19. The method as claimed in claim 12, wherein the second insulating layer is a stacked layer comprising a boro-phospho silicate glass (BPSG) layer and a tetraethylorthosilicate (TEOS) layer.

20. The method as claimed in claim 19, wherein formation of the BPSG comprises depositing a BPSG material on the passivation layer and polishing the BPSG material until the passivation layer is exposed.

21. The method as claimed in claim 19, wherein the thickness of the BPSG layer is about 5900~7300Å, and the thickness of the TEOS layer is about 3600~4400Å.

22. The method as claimed in claim 12, wherein the material of the metal layer comprises tungsten (W).

23. A structure for a bit line contact hole, comprising:

a substrate;

a transistor, disposed on the substrate, comprising

a gate layer covered by a first insulating layer and a doped region;

an inner landing pad, disposed on the doped region and parts of the transistor, comprising a polysilicon layer;

a passivation layer, disposed on the inner landing pad, the transistor, and the substrate;

a second insulating layer, disposed on the passivation layer, having a flat surface on the passivation layer;

a contact plug, disposed on the second insulating layer and the passivation, electrically connecting with the inner landing pad; and

an interconnected landing pad, deposited on the contact plug.

24. The structure as claimed in claim 23, wherein thickness of the polysilicon of the inner landing pad is about 100~400Å.

25. The structure as claimed in claim 23, wherein the material of the passivation comprises silicon nitride.

26. The structure as claimed in claim 25, wherein thickness of the passivation is about 110~130Å.